

AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A flip-flop circuit comprising
input terminals to provide a differential clock signal;
output terminals to provide a differential output signal;
differential amplifiers, each of the differential amplifiers comprising at least two transistors, the transistors comprising collectors, each collector being part of one of plural series circuits containing a resistor, the series circuits being positioned between a power supply potential terminal and a first shared emitter node and/or a second shared emitter node, sets of the collectors being interconnected to form a D flip-flop structure, the output terminals being at an output of at least one differential amplifier;
a first current source to connect the first shared emitter node to a reference potential terminal;
a second current source to connect the second shared emitter node to the reference potential terminal;
a first switch directly connected to the power supply potential terminal and directly connected to the first shared emitter node, the first switch having a first control terminal that comprises part of the input terminals; and

a second switch directly connected to the supply potential terminal and directly connected to the second shared emitter node, the second switch having a second control terminal that comprises part of the input terminals.

2. (Previously Presented) The flip-flop circuit of claim 1, wherein the differential amplifiers comprise:

a first differential amplifier comprising a first pair of emitter-coupled transistors connected to the first shared emitter node, the first pair of emitter-coupled transistors comprising collector terminals that form at least parts of a first circuit node and a second circuit node, the first pair of emitter-coupled transistors comprising base terminals that are cross-connected to collector terminals;

a second differential amplifier comprising a second pair of emitter-coupled transistors connected to the second shared emitter node, the second pair of emitter-coupled transistors comprising collector terminals that are connected to the first circuit node and/or to the second circuit node, the second pair of emitter-coupled transistors comprising base terminals that form at least part of a third circuit node and a fourth circuit node;

a third differential amplifier comprising a third pair of emitter-coupled transistors connected to the second shared emitter node, the third pair of emitter-coupled transistors comprising collector terminals that are connected to the third circuit node and/or to the fourth circuit node, the third pair of emitter-coupled transistors comprising base terminals that are cross-connected to collector terminals; and

a fourth differential amplifier comprising a fourth pair of emitter-coupled transistors connected to the first shared emitter node, the fourth pair of emitter-coupled transistors comprising collector terminals that are connected to the third circuit node and/or to the fourth circuit node, the fourth pair of emitter-coupled transistors comprising base terminals that are connected to the second circuit node and/or to the first circuit node.

3. (Previously Presented) The flip-flop circuit of claim 2, wherein the first, the second, the third, and the fourth circuit nodes are each connected via a resistor in a series circuit to the power supply potential terminal.

4. (Previously Presented) The flip-flop circuit of claim 2, wherein the first, the second, the third, and the fourth differential amplifiers and the first and the second switches are implemented using bipolar circuit technology.

5. (Previously Presented) The flip-flop circuit of claim 1, wherein the first current source and the second current source each comprise a transistor implemented using metal oxide semiconductor circuit technology.

6. (Previously Presented) The flip-flop circuit of claim 1, wherein the flip-flop circuit is implemented in emitter-coupled logic circuit technology.

7. (Previously Presented) A shift register comprising the flip-flop circuit of claim 1.

8. (Canceled)

9. (Currently Amended) A flip-flop circuit comprising:

input terminals to provide a clock signal;

output terminals to provide an output signal,

a first differential amplifier comprising first emitter-coupled transistors having emitters connected to a first emitter node, the first emitter-coupled transistors comprising collector terminals that form at least parts of a first circuit node and a second circuit node, the first emitter-coupled transistors comprising base terminals that are cross-connected to collector terminals of the first emitter-coupled transistors;

a second differential amplifier comprising second emitter-coupled transistors having emitters connected to a second emitter node, the second emitter-coupled transistors comprising collector terminals that are connected to the first circuit node and/or to the second circuit node, the second emitter-coupled transistors comprising base terminals that form at least part of a third circuit node and a fourth circuit node;

a third differential amplifier comprising third emitter-coupled transistors having emitters connected to the second emitter node, the third emitter-coupled transistors comprising collector terminals that are connected to the third circuit node and/or to the fourth circuit node, the third

emitter-coupled transistors comprising base terminals that are cross-connected to collector terminals of the third emitter-coupled transistors; and

a fourth differential amplifier comprising fourth emitter-coupled transistors having emitters connected to the first emitter node, the fourth emitter-coupled transistors comprising collector terminals that are connected to the third circuit node and/or to the fourth circuit node, the fourth emitter-coupled transistors comprising base terminals that are connected to the second circuit node and/or to the first circuit node;

a reference potential that is connectable to the first emitter node and to the second emitter node;

a first switch directly connected to a power supply potential terminal and directly connected to the first emitter node, the first switch having a first control terminal that comprises part of the input terminals; and

a second switch directly connected to the supply potential terminal and directly connected to the second emitter node, the second switch having a second control terminal that comprises part of the input terminals.

10. (Previously Presented) The flip-flop circuit of claim 9, wherein the first, the second, the third, and the fourth circuit nodes are each connected via a resistor in a series circuit to the power supply potential terminal.

11. (Previously Presented) The flip-flop circuit of claim 9, wherein the first, the second, the third, and the fourth differential amplifiers and the first and the second switches are implemented using bipolar circuit technology.

12. (Previously Presented) The flip-flop circuit of claim 9, further comprising:
a first current source to connect the first emitter node to the reference potential terminal;
and
a second current source to connect the second emitter node to the reference potential terminal.

13. (Previously Presented) The flip-flop circuit of claim 12, wherein the first current source and the second current source each comprise a transistor implemented using metal oxide semiconductor circuit technology.

14. (Previously Presented) The flip-flop circuit of claim 9, wherein the flip-flop circuit is implemented in emitter-coupled logic circuit technology.

15. (Previously Presented) A shift register comprising the flip-flop circuit of claim 9.

16. (Canceled)